## <u>REMARKS</u>

Claims 1-10 were examined, and all claims are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dao et al. (U.S. Patent No. 6,275,891) in view of Lowe et al. (U.S. Patent No. 6,173,243). Applicant respectfully traverses this rejection for the reasons set forth below.

The present invention is directed to a signal processing apparatus having a channel pooling signal processor 76 and a digital signal processor (DSP) 72, wherein the channel pooling signal processor 76 performs more computationally intensive signal processing operations than the DSP 72. The channel pooling signal processor 76 has computation units 36, a test interface 34 for testing the function of the computation units 36, a microprocessor 74 for managing data flow into and out of the channel pooling signal processor 76, and an interconnect mechanism 32 for connecting the computation units 36, the interface 34, and the microprocessor 74.

The applied references do not suggest the claimed channel pooling signal processor, which is a specialized processor that is reconfigurable and designed to perform intensive mathematical processing. As claimed, and as shown in Figs. 2-5, the channel pooling signal processor 76 includes computation units 36, a test interface 34, a microprocessor 74, and an interconnect mechanism 32. The computation units 36 are located within a heterogeneous reconfigurable multiprocessor 66.

Dao discloses a processing architecture in which a hardware accelerator is coupled to a DSP 108 and a DSP memory 110 via a DSP bus 112. The DSP 108 performs less demanding computationally-intensive tasks of pre-processing and post-processing data, and allows the hardware accelerator to perform processing steps that the DSP 108 is too inefficient to perform. Col. 1, line 61, to col. 2, line 12.

Contrary to the Examiner's assertion, Dao's hardware accelerator is not equivalent to the claimed channel pooling processor, which includes a plurality of computation units. There is virtually no disclosure in Dao as to what is included in its hardware accelerator. That is, there is no disclosure or suggestion in Dao that the hardware accelerator includes a plurality of computation

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units. The claimed computation units perform computationally intensive operations, such as channel decoding, equalization, chip-rate processing, synchronization, channelization, parameter estimation, etc. (See specification, page 7, lines 13-25.) Since Dao does not suggest computation units, Dao does not suggest the claimed channel pooling signal processor. Thus, the claims are patentable over the applied references for at least this reason.

With further regard to claims 3-5, there is no disclosure or suggestion in Dao of a second channel pooling signal processor (claim 3), or that the computation units are heterogeneous (claim 4) or homogeneous (claim 5). Thus, claims 3-5 are patentable for these additional reasons.

Further, claim 9 is specifically directed to a base station transceiver. There is no disclosure or suggestion in the applied references, alone or in combination, of a base station transceiver. Claim 9 is therefore further patentable for this additional reason.

Newly added dependent claims 11-22 are directed to further details of the computation units. More specifically, the new claims recite that the computation units are flexibly configured and connected to perform any one of several different transceiver functions (claims 11, 14, 17, and 20), are configured to perform one or more of downconversion, dechannelization, demodulation, decoding, equalization, despreading, encoding, modulation, spreading, and diversity processing (claims 12, 15, 18, and 21), and support time-division, code-division, and/or frequency division processing (claims 13, 16, 19, and 22). The applied references do not teach or suggest any of these features, and thus these claims are patentable over the applied references for these additional reasons.

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In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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